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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP 2101 L Street, NW Washington, DC 20037			EXAMINER WERNER, BRIAN P	
			ART UNIT 2621	PAPER NUMBER

DATE MAILED: 09/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/516,581

Applicant(s)

DELAROSA ET AL

Examiner

Brian P. Werner

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 June 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,3-14,16-27 and 29-39 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 3-14, 16-27 and 29-39 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Response to Amendment*

1. The amendment and response received on June 30, 2005 has been entered. Claims 1, 3-14, 16-27 and 29-39 remain pending.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 14 and 27 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Barr et al. (US 5,776,645 A). Refer to figure 3, figure 24 and column 14, line 48 to column 15, line 12. Figure 3 depicts the apparatus and figure 24 depicts the method performed by the apparatus in the embodiment that corresponds to the applicant's claimed invention.

Barr discloses a system for determining the relative location of an upper and lower layer of an integrated circuit (see "a fifth aspect ..." at column 3, line 15, as well as figures 3 and 24, and column 14, line 48 to column 15, line 12), comprising comparing said relative location to

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stored acceptable design limits (“From the results of the overlay determination, the registration of the print bias target with respect to the lower level image is found. The resultant overlay coordinate may then be compared to tolerances specified in a given situation to determine whether the overlay is within acceptable parameters” at column 15, line 10; this embodiment as is all other embodiments of the Barr reference are performed by the structure depicted in figure; that is, Barr states, “FIG. 3 is a block diagram of an exemplary imaging system, in this case projection imaging system 150, and print bias measuring tool 152 useful in performing the various methods of the present invention with respect to, for example, semiconductor wafers” at column 5, line 64).

Barr teaches determining a location of a first feature reference point in said visible feature of one of said layers, and a location of a second feature reference point in said visible feature of the other of said layers, to indicate a relative location (“A center of the prior-level image is determined, along with an average center for the print bias target. After the center and average center are determined, a location of the average center relative to the center is determined, thereby determining the overlay. The print bias target may comprise a pair of concentric geometric shapes. The average center thereof being determined by finding a midpoint between corresponding sides of the concentric geometric shapes, treating the collection of midpoints on all sides of the concentric geometric shapes as an intermediate shape, the center of which is the average center for the print bias target” at column 3, lines 20-30).

***Claim Rejections - 35 USC § 103***

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4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 1, 3-9, 11-14, 16-22, 24-27, 29-35 and 37-39 rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Into (US 4,938,600 A) and Barr et al. (US 5,776,645 A).

### **The Into Reference**

Regarding claim 1, which is representative of claim 27, Into discloses a method for measuring the registration between two integrated circuit layers, one residing over the other (“methods and apparatus for measuring the registration between overlying layers of a semiconductor wafer” at column 1, line 10), comprising:

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generating a top-down image of a field of view of the two integrated circuit layers (figures 1 and 2, numeral 22; “camera 22 have a vertical optical axis” at column 4, line 7), each of the layers having a respective visible feature in the image (figures 3A-4B; e.g., figure 4A, numeral 70 is a visible feature on a first layer, and numeral 72 is a visible feature on a second layer; refer to column 6, lines 20-23);

digitizing the image and processing the digitized image (“electrical signals representative of the image are supplied to an image processor 28 and a computer 30” at column 4, line 15; “computer 30 processes the signals from the camera 22” at column 4, line 24; The computer is performing the measurement, and thus the signals must be digitized) to determine a relative location of the visible feature of one layer relative to the feature of the other layer (e.g., figure 4A, numerals 70a and 72a each correspond to the center points of the squares 70 and 72; refer to column 6, line 24; see also “to measure displacement between layers of the semiconductor wafer 16” at column 4, line 26; “by measuring the displacement of patterns 50 and 54, the registration between layers 52 and 56 can be quantified” at column 4, line 44);

determining a location of a first feature reference point in said visible feature of one of said layers, and a location of a second feature reference point in said visible feature of the other of said layers, to indicate a relative location (in figures 4A and 4B, a center point 70a is determined for feature 70 of a first layer, and a center point 72a is determined for feature 72 of the second layer; see “the center of pattern 70 is shown at 70a , and the center of pattern 72 is shown at 72a” at column 6, line 24; it if from these center points that the “displacements” are calculated as described at column 6, line 27 and depicted in figures 4A and 4B: NOTE: Applicant also discloses utilizing center points of visible features as “feature reference points” at

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depicted in applicant's figure 4, and described in the applicant's specification at page 19, line 19 which states, "... image from image processor 148 and finds the center points 305 and 307 of the respective features 301 and 303 of the two overlapping material layers."; This is exactly what Into teaches at figures 4A and 4B, where the center points of features 70 and 72 are determined, from which an offset can be calculated); and

determining if the relative location is within acceptable design limits for the integrated circuit layers ("acceptable tolerances on displacement between layers" at column 1, line 28; "outside tolerable limits" at column 1, line 47).

Regarding claim 14, Into discloses an apparatus corresponding to the apparatus disclosed by the applicant with the exception below.

Regarding claims 3-5, 16-18 and 29-31, x and y locations of first and second feature reference points are found (e.g., figure 4A, numerals 70a and 72a), from which delta-x and delta-y displacement is measured (figure 4A, "X1" and "Y1"; "x-axis displacement" and "y-axis displacement" at column 6, lines 26-27; a "displacement" as defined by Into is, for example, a "displacement of the squares [or other features] relative to each other" at column 1, line 40; given the situation of figure 4A, where the location of square centers 70a and 72a are determined, from which a displacement is calculated, it necessarily follows that the displacement is a subtraction of x and y values of the coordinates of the square centers).

Regarding claims 6-8, 19-21, and 32-34, Into discloses comparing the relative location with stored tolerance limits (as described in the claim 1 rejection), including calculating an offset value (figure 4A, "X1" and "Y1"; "x-axis displacement" and "y-axis displacement" at column 6, lines 26-27; a "displacement" as defined by Into is, for example, a "displacement of the squares

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[or other features] relative to each other” at column 1, line 40; given the situation of figure 4A, where the location of square centers 70a and 72a are determined, from which a displacement is calculated, it necessarily follows that the displacement is an offset of one square from the other) and comparing the offset to a predetermined tolerance (“verify registration” and “if the displacement is outside tolerable limits” at column 1, lines 45-48).

Regarding claims 9, 11, 12, 22, 24, 25, 35, 37 and 38, an imaging system is disclosed comprising a video camera and a microscope (figure 2, numerals 20 and 22).

Regarding claims 13, 26 and 39, semiconductor layers are disclosed (layers of a semiconductor wafer” at column 1, line 10).

### **Differences**

While Into teaches determining if the relative location is within acceptable design limits for the integrated circuit layers (“acceptable tolerances on displacement between layers” at column 1, line 28; “outside tolerable limits” at column 1, line 47), Into does not teach “comparing said relative location to said stored acceptable design limits” as now required by independent claims 1 and 27. In addition, Into does not teach the corresponding structure of “means for determining if said relative location is within acceptable design limits” as required by independent claim 14 (i.e., the corresponding structure being a computer or processor and its associated support circuitry as depicted in applicant’s figure 2, numeral 150).



**The Barr Reference**

Barr discloses a system for determining the relative location of an upper and lower layer of an integrated circuit (see “a fifth aspect ...” at column 3, line 15, as well as figures 3 and 24, and column 14, line 48 to column 15, line 12), comprising comparing said relative location to stored acceptable design limits (“From the results of the overlay determination, the registration of the print bias target with respect to the lower level image is found. The resultant overlay coordinate may then be compared to tolerances specified in a given situation to determine whether the overlay is within acceptable parameters” at column 15, line 10; this embodiment as is all other embodiments of the Barr reference are performed by the structure depicted in figure; that is, Barr states, “FIG. 3 is a block diagram of an exemplary imaging system, in this case projection imaging system 150, and print bias measuring tool 152 useful in performing the various methods of the present invention with respect to, for example, semiconductor wafers” at column 5, line 64).

**The Barr and Into Combination**

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Into’s step of determining whether the relative location is within acceptable design limits for the integrated circuit layers (“acceptable tolerances on displacement between layers” at column 1, line 28; “outside tolerable limits” at column 1, line 47), by performing a comparison of the relative location to stored acceptable design limits as taught by Barr, in order to “determine whether the overlay is within acceptable parameters” (Barr column 15, line 11) by virtue of a simple comparison operation, not requiring operator intervention or complex

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processing, and further providing the ability to adapt the acceptable design limits (i.e., Barr's tolerances) to different situations such as different types of circuit boards, and to circuits that are either more or less sensitive to deviations of their layers ("specified in a given situation", Barr, column 15, line 11).

7. Claims 10, 23 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Into (US 4,938,600 A) and Barr et al. (US 5,776,645 A), and further in combination with Seiler et al. (US 4,766,311 A).

The Into and Barr combination does not teach a scanning electronic microscope.

Seiler discloses a system that captures images of wafers, where the image scanner is a scanning electron microscope ("scanning electron microscopes" at column 2, line 60).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to utilize the electron microscope of Seiler as the image pickup device required by Into to capture images that are "highly precise" (Seiler, column 1, line 10).

### ***Response to Arguments***

8. Each of the remarks and/or arguments filed with the aforementioned amendment have been considered:

The Barr Reference:

Summary of Applicant's Remarks: "Thus, Barr discloses calculating an average measurement or 'average center' between two features, and not 'determining a location of a first feature reference point in said visible feature of one of said layers'" at response page 9.

Examiner's Response: Disagreed. Barr's average center is, ultimately, a single point within the feature and that is all that is called for by the claim.

Independent claim 1, which is representative of independent claims 14 and 27, requires "determining a location of a first feature reference point in said visible feature of one of said layers". Thus, the claim requires the determination of a "first feature reference point", and that point must be "in said visible feature".

Barr teaches that "a center of the prior-level image is determined, along with an average center for the print bias target", where the "average center thereof being determined by finding a midpoint between corresponding sides of the concentric geometric shapes, treating the collection of midpoints on all sides of the concentric geometric shapes as an intermediate shape, the center of which is the average center for the print bias target" at column 3, lines 20-30.

Thus, Barr teaches the determination of a single "point" that is within the visible feature (i.e., at the center). That fact that Barr uses an averaging process to determine the point location is not precluded by the open ended claim.

Furthermore, Barr's finding of a center point is consistent with the applicant's own specification. That is, applicant discloses utilizing center points of visible features as "feature reference points" as depicted in applicant's figure 4, and described in the applicant's specification at page 19, line 19 which states, "... image from image processor 148 and finds the

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center points 305 and 307 of the respective features 301 and 303 of the two overlapping material layers.” Thus, Barr meets the broadly recited claim limitation of determining a feature point within the visible feature, as well as the applicant’s disclosed embodiment of determining a “center point” within the feature.

The Into and Barr Combination:

Summary of Applicant’s Remarks: “In particular, Into and Barr, even when considered together, fail to teach or suggest ‘determining a location of a first feature reference point in said visible feature of one of said layers, and a location of a second feature reference point in said visible feature of the other of said layers’” at response pages 10-11.

Examiner’s Response: Disagreed. Into teaches in figures 4A and 4B, that a center point 70a is determined for feature 70 of a first layer, and a center point 72a is determined for feature 72 of the second layer (“the center of pattern 70 is shown at 70a , and the center of pattern 72 is shown at 72a” at column 6, line 24). It is from these center points that the “displacements” are calculated as described at column 6, line 27 and depicted in figures 4A and 4B.

Summary of Applicant’s Remarks: “In particular, Into and Barr, even when considered together, fail to teach or suggest ... ‘determining if said relative location is within stored acceptable design limits for said integrated circuit layers by comparing said relative location to said stored acceptable design limits’” at response page 11.

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Examiner's Response: Disagreed. Into teaches that the purpose of determining the displacements between the layers is to ensure that they meet "acceptable tolerances on displacement between layers" at column 1, line 28 (see "outside tolerable limits" at column 1, line 47). While Into teaches determining if the relative location is within acceptable design limits for the integrated circuit layers, Into does not teach "comparing said relative location to said stored acceptable design limits". This is exactly what Barr teaches as described above. That is, Barr discloses a system for determining the relative location of an upper and lower layer of an integrated circuit (see "a fifth aspect ..." at column 3, line 15, as well as figures 3 and 24, and column 14, line 48 to column 15, line 12), comprising comparing said relative location to stored acceptable design limits ("From the results of the overlay determination, the registration of the print bias target with respect to the lower level image is found. The resultant overlay coordinate may then be compared to tolerances specified in a given situation to determine whether the overlay is within acceptable parameters" at column 15, line 10. Thus, the Into and Barr combination fully meet the claimed requirements.

Summary of Applicant's Remarks: "Into does not teach or suggest the actual method of measuring displacement" at response page 11.

Examiner's Response: Disagreed. Into states, "any registration error produces a displacement of the squares relative to each other" at column 1, line 40, and Into measures the displacement as depicted in figures 4A and 4B, indicated by "X1", "Y1", "X2" and "Y2".

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Summary of Applicant's Remarks: "... the Into method only teaches a new method to eliminate systematic errors ... and not a 'method for measuring the registration between at least two integrated circuit layers'" at response page 11.

Examiner's Response: Refer to the title of the Into patent, which reads, "METHOD AND APPARATUS FOR MEASURING REGISTRATION BETWEEN LAYERS OF A SEMICONDUCTOR WAFER".

The remainder of the arguments has been addressed by the examiner hereinabove.

### ***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hopkins (US 4,989,082 A) is relevant as teaching a method of determining whether a relative location of an upper and lower layer are within an acceptable tolerance, where the tolerance is stored (figure 5; "The acceptability or not is determined by a comparator 59. When counting is complete, a read signal applied to the counters 57 and 58 causes the latter to input their respective counts to the comparator 59. In known manner, the comparator compares the difference between X1 and X2 with the tolerance dX, and generates an error signal if the difference exceeds this tolerance" at column 8, line 20). This reference can, and may be equally applied to the Into reference in the same manner as Barr above.

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10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Werner whose telephone number is 571-272-7401. The examiner can normally be reached on M-F, 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Mancuso can be reached on 571-272-7695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Werner  
Primary Examiner  
Art Unit 2621  
9/12/2005



**BRIAN WERNER**  
**PRIMARY EXAMINER**